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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/675,778
Filing Date: September 30, 2003
Appellant(s): DEWITT ET AL.

Gerald H. Glanzman
Reg. No. 25,035
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 29 September 2006 appealing from the Office action mailed 31 May 2006.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

No amendment after final has been filed.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claim Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

Davidson, U.S. Patent No. 6,446,029

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-2, 4-25 are rejected under 35 U.S.C. 102(b) as being anticipated by Davidson et al. (U.S. Patent No. 6,446,029) hereinafter referred to as Davidson.

As per claim 1, Davidson discloses a method in a data processing system for processing instructions, the method comprising: responsive to receiving an instruction at a processor in the data processing system, determining whether an indicator is associated with the instruction (Col. 7 line 64 - Col. 8 line 32), wherein a threshold value is located in the indicator (Fig. 5B threshold registers 521-525); and counting executions of the instruction if the indicator is associated with the instruction and if a time for executing the instruction exceeds the threshold value (Col. 8 lines 61-65). *The examiner asserts that, as described in col. 7 line 64 – col. 8 line 32, the instruction tag and the threshold value registers collectively comprise the "indicator". As such, the indicator contains the threshold values.*

As per claim 2, Davidson discloses the method of claim 1, wherein the counting step comprises:

determining whether the time to execute the instruction exceeds the threshold value; (Col. 8 lines 61-65)

generating, by an instruction cache, a signal indicating that executions of the instruction are to be counted if a determination is made that the time for executing the instruction exceeds the threshold value; (tagged instructions, col. 7 line 64 – col. 8 line 32) *The examiner asserts that logic block generating the tag constitutes a portion of the instruction cache as at least one instruction is temporarily held there before executing.*

receiving the signal generated by the instruction cache at a performance monitor unit; and incrementing a counter in the performance monitor unit each time the instruction is executed in response to receiving the signal from the instruction cache. (Col. 5 line 38-40)

As per claim 4, Davidson discloses the method of claim 1, wherein the indicator is located in a shadow memory. *The examiner asserts that the tag resides in memory. If it did not, the processor would have no way to know which instructions are to be monitored and which are not.*

As per claim 5, Davidson discloses the method of claim 1, wherein the instruction is received in a bundle and wherein the indicator comprises at least one spare bit in a field in the bundle. *The examiner asserts that the processor is capable of executing*

multiple instructions per clock cycle (Col. 5 lines 1-2), further, a bundle may only encompass a single instruction. The examiner asserts that as soon as an instruction is tagged (col. 7 line 64 – col. 8 line 32), the tag is encompassed in the instruction bundle.

As per claim 6, Davidson discloses the method of claim 1, wherein the counting step comprises:

determining whether the time to execute the instruction exceeds the threshold value; (Col. 8 lines 59-65)

generating, by an instruction cache, a signal indicating an interrupt is present if a determination is made that the time for executing the instruction exceeds the threshold value; *Examiner asserts that thresholder 520 generates a signal indicating a count should occur.* (Col. 8 lines 59-65)

receiving the signal generated by the instruction cache at an interrupt unit; and executing code, by the interrupt unit, to count each execution of the instruction. (Col. 8 lines 59-66)

As per claim 7, Davidson discloses the method of claim 6, wherein the code also gathers information from a call stack (Fig. 6A completion table 600) for the instruction. (Col. 9 lines 25-33) *Threshold values 605 are transferred to the threshold registers and used in determining whether to count or not.*

As per claim 8, Davidson discloses the method of claim 1, wherein the threshold is a number of clock cycles. *Inherently, the interval values stored in threshold registers must be multiples of clock cycles as a processor uses a clock to determine all timing requirements.*

As per claim 9, Davidson discloses a method in a data processing system for processing instructions, the method comprising: receiving an initial instruction at a processor in the data processing system, wherein the initial instruction indicates that counting execution of a subsequent instruction occurs if a time to execute the subsequent instruction exceeds a threshold value located in the initial instruction; and counting executions of the subsequent instruction if the time to execute the subsequent instruction exceeds the threshold value. (Col. 11 lines 17-20) *The examiner asserts that in order to load/store a threshold value directly to the thresholder, a first instruction must occur, as the processor cannot operate without an instruction to tell it what to do. That load/store instruction must inherently contain the threshold value to be compared to.*

As per claim 10, Davidson discloses the method of claim 9, wherein the counting step comprises:

determining whether the time to execute the subsequent instruction exceeds the threshold value; (Col. 8 lines 59-65)

generating, by an instruction cache, a signal indicating that each execution of the subsequent instruction is to be counted if a determination is made that the time for executing the subsequent instruction exceeds the threshold value; (Col. 8 lines 59-65)

receiving the signal generated by the instruction cache at a performance monitor unit; and incrementing a counter in the performance monitor unit each time the subsequent instruction is executed in response to receiving the signal from the instruction cache. (Col. 8 lines 59-66)

As per claim 11, Davidson discloses a method in a data processing system for processing data, the method comprising: responsive to a request to access data, determining whether an indicator is associated with the data (Col. 7 line 64 - Col. 8 line 32), wherein a threshold value is located in the indicator (Fig. 5B threshold registers 521-525); and counting access to the data if the indicator is associated with the data and if a time needed to access the data exceeds the threshold value. (Col. 8 lines 61-65) *The examiner asserts that a load/store instruction has an indicator associated with it and the instruction is associated with the data it is accessing, therefore the indicator is also associated with the data. When the instruction in question is a load/store instruction (Col. 6 lines 12-14) comparing the threshold for execute stage will tell if the load/store was accomplished in a time greater than the threshold value. The examiner asserts that, as described in col. 7 line 64 – col. 8 line 32, the instruction tag and the threshold value registers collectively comprise the "indicator". As such, the indicator contains the threshold values.*

As per claim 12, Davidson discloses the method of claim 11, wherein the counting step comprises: generating an exception if the indicator is associated with the data and if the time to access the data exceeds the threshold value. *The examiner asserts that a signal is generated by the thresholder upon detection* (Col. 8 lines 59-65)

As per claim 13, Davidson discloses the method of claim 11, wherein the counting step comprises:

determining whether the time to access the data exceeds the threshold value; (Col. 8 lines 59-65)

generating, by a data cache, a signal indicating that accesses of the data are to be counted if a determination is made that the time for accessing the data exceeds the threshold value; (Col. 8 lines 59-65) *The examiner asserts that thresholder constitutes a data cache, as data is temporarily stored therein.*

receiving the signal generated by the data cache at a performance monitor unit; and incrementing a counter in the performance monitor unit each time the data is accessed in response to receiving the signal from the data cache. (Col. 8 lines 59-66)

As per claim 14, Davidson discloses the method of claim 11, wherein the counting step comprises:

determining whether the time to access the data exceeds the threshold value; (Col. 8 lines 59-65)

generating, by a data cache, a signal indicating an interrupt is present if a determination is made that the time for accessing the data exceeds the threshold value; (Col. 8 lines 59-65) *The examiner asserts that thresholder constitutes a data cache, as data is temporarily stored therein. Further, the signal generated by the thresholder constitutes an interrupt.*

receiving the signal generated by the data cache at an interrupt unit; and executing code, by the interrupt unit, to count accesses of the data. (Col. 8 lines 59-65)

As per claim 15, Davidson discloses the method of claim 11, wherein the data is located in a memory location. *The examiner asserts the data being accessed in a load or store is located in a memory location.*

As per claim 16, Davidson has taught a processing system performing the method of claim 1, consequently claim 16 is rejected for the same reasons set forth in the rejection of claim 1 above.

As per claim 17, Davidson has taught a processing system performing the method of claim 2, consequently claim 17 is rejected for the same reasons set forth in the rejection of claim 2 above.

As per claim 18, Davidson has taught a processing system performing the method of claim 6, consequently claim 18 is rejected for the same reasons set forth in the rejection of claim 6 above.

As per claim 19, Davidson has taught a processing system performing the method of claim 9, consequently claim 19 is rejected for the same reasons set forth in the rejection of claim 9 above.

As per claim 20, Davidson has taught a processing system performing the method of claim 10, consequently claim 20 is rejected for the same reasons set forth in the rejection of claim 10 above.

As per claim 21, Davidson has taught a processing system performing the method of claim 11, consequently claim 21 is rejected for the same reasons set forth in the rejection of claim 11 above.

As per claim 22, Davidson has taught a processing system performing the method of claim 12, consequently claim 22 is rejected for the same reasons set forth in the rejection of claim 12 above.

As per claim 23, Davidson has taught a computer program product in a computer readable medium (Col. 12 line 62 – Col. 13 line 6) performing the method of claim 1,

consequently claim 23 is rejected for the same reasons set forth in the rejection of claim 1 above.

As per claim 24, Davidson has taught a computer program product in a computer readable medium (Col. 12 line 62 – Col. 13 line 6) performing the method of claim 9, consequently claim 24 is rejected for the same reasons set forth in the rejection of claim 9 above.

As per claim 25, Davidson has taught a computer program product in a computer readable medium (Col. 12 line 62 – Col. 13 line 6) performing the method of claim 11, consequently claim 25 is rejected for the same reasons set forth in the rejection of claim 11 above.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Davidson.

As per claim 3, Davidson discloses the method of claim 1, wherein the threshold value is stored in the indicator but fails to disclose wherein the threshold value is a three-bit value.

Using three bits to represent the threshold value would be beneficial in that a small amount of logic is needed to represent the value and up to eight different values can be produced.

It would have been obvious to one of ordinary skill in the art at the time of invention to have included three bits in the representation of the threshold values for the benefit of allowing eight different values with a small amount of logic. Further, as shown in In re Rose, 105 USPQ 237 (CCPA 1955) changes in size/range are generally not given patentable weight or would have been obvious improvements.

(10) Response to Argument

Applicant's arguments filed 29 September 2006 have been fully considered but they are not persuasive.

Applicant states:

"Applicants respectfully submit that Davidson does not teach or suggest 'responsive to receiving an instruction at a processor in the data processing system, determining whether an indicator is associated with the instruction, wherein a threshold value is located in the indicator"

Examiner disagrees. On an Office Action dated 31 May 2006, Examiner stated the following:

"The examiner asserts that, as described in col. 7 line 64 – col. 8 line 32, the instruction tag and threshold value registers [located at fig. 5B reference 521-525] collectively comprise the 'indicator'. As such, the indicator contains the threshold values."

Examiner made this statement to preemptively clarify the issue that is currently up for debate. Applicant does not agree that the tag and threshold values can collectively be considered an indicator. Applicant states: "The threshold values are not located in an indicator associated with an instruction as required by claim 1, and there is nothing in the above paragraphs or anywhere else in Davison that would suggest or support such an interpretation."

It appears that Applicant believes that these two elements cannot be collectively interpreted as an indicator simply because Davison does not use the term "indicator" when addressing these terms. Examiner disagrees. Applicant's indicator "may take various forms and may take various sizes depending on the particular implementation." See Applicant's Specification page 27 lines 4-6. Applicant's invention and the teachings of Davison both disclose an indicator (as being interpreted by the Office Action) as a short series of bits. Additionally, The fact that Davidson gives the names "threshold register" and "instruction tag" does not change the fact that these bits complete the same functionality as claimed by Applicant. Applicant's Specification on page 27 clearly describes indicators being used in the same way as Davidson's instruction tag and threshold registers; "[a] single bit may be used to indicate that events are to be counted in response to execution of that instruction"; "[m]ultiple bits may be used to identify a threshold."

Consequently, even if Examiner chose to read several significant limitations from Applicant's Specification into the claims (which Examiner believes is unreasonable), the teachings of Davidson still adequately anticipate this limitation of Applicant's invention.

Applicant states:

"Davidson fails to teach 'counting executions of the instruction if the indicator is associated with the instruction and if a time for executing the instruction exceeds the threshold value. . . At best, [Davidson col. 8 lines 59-66] may disclose counting 'a threshold event signal' which is asserted 'if an instruction pipeline requires more time to complete than indicated by its corresponding threshold value"

Examiner disagrees. Davidson col. 8 lines 59-66 discloses the following:

"Thresholder 520 monitors the stage completion signals and compares the stage completion signals and compares time intervals of each pipeline stage with threshold values stored in threshold registers 521-525. If an instruction pipeline stage requires more time to complete than indicated by its corresponding threshold value, then thresholder 520 asserts a threshold event signal 526 that is collected by an event counter or multiple event counters 530 in the performance monitor."

Applicant's Specification on page 35 states:

"A determination is made as to whether the threshold has been exceeded for this instruction. If a threshold has been exceeded, then a selected action is performed. This selected action may take different forms depending on the particular implementation. For example, a counter may be incremented each time the threshold is exceeded."

Examiner fails to see a significant distinction that Applicant is arguing. Both Davidson and Applicant's Specification disclose a threshold value being exceeded and, as a result, updating a counter. And even if subtle distinctions exist within the specification, the disclosure of Davidson certainly anticipates the limitation as claimed: "counting executions of the instruction if the indicator is associated with the instruction and if a time for execution the instruction exceeds the threshold value."

Applicant appears to argue that the distinction lies within Davidson's counting of a signal rather than counting the event of exceeding a threshold value. Examiner finds this argument unpersuasive. The "threshold event signal 526" disclosed in Davidson is the mechanism used to update the counter based on an exceeded threshold value. This is how processor elements communicate—using signals.

Consequently, these limitations of Applicant's claimed invention are properly anticipated by the disclosure of Davidson.

Applicant states:

"Furthermore, claim 1 specifically recites 'responsive to receiving an instruction at a processor in the data processing system, determining whether an indicator is associated with the instruction, wherein a threshold value is located in the indicator." Even if the instruction tag and the threshold value registers in Davidson can somehow be construed as collectively comparing an indicator, there is never any determination made in Davidson as to whether the threshold registers are associated with instructions which flow through the pipeline units in Davidson which would appear necessary if the indicators includes the threshold registers. The threshold registers are always present in Davidson and making such a determination would be meaningless at the very least"

Examiner disagrees. It is unclear what definition of "determining" Applicant is using. The application under debate is concerning a processor. Any determining that is done is far from a rational thought process; it is simply a cause and effect relationship. Dictionary.com defines "determine" as "to come to a decision or resolution." This appears to be a fair definition when instruction-processing systems are concerned.

Consequently, for the disclosure of Davidson to appropriately anticipate Applicant's claims, Davidson is required to determine (come to the resolution that) an indicator is associated with an instruction in response to receiving the instruction. While remembering that, as interpreted in the Office Action filed 31 May 2006, the instruction tag of Davidson is part of the claimed indicator, Davidson col. 7 line 64 to col 8 line 32 adequately discloses this determination in detail. In particular, Examiner directs attention to the following:

"As an instruction is fetched, a single instruction may be selected and marked (or tagged)...Instructions may be marked based on a variety of selection mechanism, each of which may be under the control of the performance monitor. An instruction may be selected at random, in which case the performance monitor may capture the instruction address after the instruction has been randomly selected, e.g., by receiving instruction address 509 from fetch unit 501. And instruction may be selected based on a general category of its instruction type, such as any store instruction. A specific type of

instruction may be selected, such as a load instruction that uses particular registers. As another alternative, an instruction may be selected based on its instruction address, which provides functionality for debugging program to store specific instructions at specific addresses and then to allow the processor to execute the instructions without setting interrupts or traps. The above list merely provides some examples and should not be considered an exhaustive list of potential instruction selection mechanism."

So, not only is it perfectly clear that Davidson does determine whether an indicator (instruction tag) is associated with an instruction responsive to receiving the instruction, Davidson gives numerous examples of how this determination is made. This limitation is clearly satisfied by the disclosure of Davidson.

Applicant states:

"Claim 3 depends from claim 1, and recites that the threshold value is a three bit value located in the indicator. In rejecting the claim, the Examiner acknowledges that Davidson fails to disclose the subject matter of claim 3, but contends that it would have been obvious to one of ordinary skill in the art at the time of the invention to have located the threshold values inside the indicator for the benefit of reduced logic. The Examiner also asserts that using three bits to represent the threshold value would be obvious because 'a small amount of logic is needed to represent the value and up to eight different values can be produced'. Appellants respectfully disagree with the Examiner's conclusions. . .[Davidson] certainly does not disclose or suggest the threshold value is a three bit value located in the indicator. . . Applicants submit that the Examiner is using hindsight based on Applicants' own disclosure to modify Davidson in an effort to achieve the present invention"

Examiner disagrees. Examiner never made the assertion that it would have been obvious to have located the threshold value inside the indicator. Davidson alone meets this limitation. An Office Action dated 31 May 2006 states "Davidson discloses the method of claim 1, wherein the threshold value is stored in the indicator." The analysis of this disclosure is adequately described in the rejection of claim 1 and with respect to the arguments presented above. Examiner did take Official Notice that it would have been obvious for the threshold value to contain a three-bit value.

In support of this assertion, Examiner cited *In re Rose*, 105 USPQ 237 (CCPA 1955) which held that changes in size/range are generally not given patentable weight or would have been obvious improvements.

Additionally, Applicant's specification suggests that the use of exactly three bits is no more than an arbitrary example. Applicant's specification states that the threshold value can be various sizes.

"Multiple bits may be used to identify a threshold, such as a number of processor or clock cycles for instruction execution that may pass before events should be counted. Further, these bits may even be used as a counter for a particular instruction. A similar use of fields may be used for indicators that mark data or memory locations." See Applicant's Specification page 27.

Applicant's disclosure of exactly three bits is on page 34 and is shown as a mere example. Nothing within this example suggests that three bits is better than any other bit value. In fact, page 34 states, "More or fewer bits may be used and different values may be assigned to the bits depending on the specific implementation." This statement supports that the use of three bits is an obvious change based on specific implementation and is not an essential for the invention. See *in re Kuhle*, 526 F.2d 553, 555, 188 USPQ 7, 9 (CCPA 1975).

Consequently, the limitations of claim 3 are obvious and are properly rejected under 35 USC 103 with respect to Davidson.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejection should be sustained.

Respectfully submitted,

Brian P. Johnson

07 December 2006

Conferences:

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